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Efficient Utilization of Channel Coding for Wireless Communication

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Abstract— *In this paper, a trade-off analysis between concatenated codes consisting of a convolutional (CC) followed by a Reed-Solomon (RS) code versus low-density parity-check (LDPC) codes is presented. The analysis is based on a twofold criterion: coding gain for a target bit error rate (BER) of 10-6 and required decoder hardware complexity for a target data throughput of 10 Gbps. Furthermore, we have investigated relevant parameters which directly impact an efficient hardware implementation as well as the error correction performance of the LDPC decoder. These parameters include an attenuation factor in the min-sum layered (MSL) decoding algorithm, the finite word length of soft information and an early-termination (ET) strategy. The error correction performances are evaluated for 16-QAM modulation over an independent Rayleigh fading channel. The complexity of the RS-CC and LDPC decoders is estimated based on synthesis results using an Infineon 40 nm CMOS design kit.*

Keywords - Reed-Solomon, LDPC, convolutional code, concatenated code, Rayleigh fading, BER performance, decoder complexity, data throughput

1. INTRODUCTION

In wireless communications, reliable and high throughput data transmission is the key feature for the commercial success of new transmission schemes. In order to protect data against transmission errors caused by channel noise, channel coding based on error correction codes is widely used. A large variety of channel codes has been developed in the last few decades including convolutional codes (CC), Reed-Solomon (RS) codes, and most recently turbo and LDPC codes. The concatenated Reed-Solomon convolutional code (RSCC) has been applied in different communication standards, e.g., IEEE 802.16e [1], ECMA-387 [2], and telemetry channel coding [3] (CCSDS standard). On the other hand, LDPC codes have been also utilized in IEEE 802.16e (WiMAX) and additionally in e.g., IEEE 802.11n [4], IEEE 802.15.3c [5] and several digital video broadcasting (DVB) standards [6]. Most of these communication standards and their different generations are typically driven by a request for ever higher data throughput. As a result, the implementation complexity of a state-of-art Forward-Error-Correction (FEC) decoder is one of the most important factors which should be considered in the development of a wireless communication system.

In this paper, we present a trade-off analysis providing performance evaluation and implementation complexity of RS-CC and LDPC decoders for multi-Gbps wireless communications. Since the performance space exploration is very large, we focus on widely used channel codes. For the concatenated RS-CC code, as an inner code, the well-known convolutional (171,133) code with constraint length of K = 7 is used. As an outer code, we use RS codes with one byte RS symbol size and a longest codeword length of 255 bytes, [1-2]. In order to further improve performance of this concatenated code, a block interleaver between the RS and CC code is considered. On the other hand, concerning LDPC coding, we adopt structured LDPC codes from the IEEE 802.16e standard. Those codes are suitable for high-speed layered decoding. Having in mind that higher order modulations are able to offer higher data throughputs, we omit BPSK and QPSK modulation and only focus on 16-QAM in this paper. We focus on an independent Rayleigh fading channel where no line-ofsight (LOS) signal component is present.

2. SYSTEM MODEL

The system model on which we base the BER performance evaluation is shown in Figure 1. At the transmitter, the input bits after channel coding are converted into QAM symbols, according to Gray-coded constellation mappings. These symbols are

transmitted over an independent Rayleigh fading channel with additive white Gaussian noise (AWGN). Let x(i) = xI(i) + jxQ(i) denote the i-th transmitted QAM symbol. Indices I and Q correspond to the in-phase and quadraturephase component, respectively. The received symbols can be written as

$$r(i) = h(i)x(i) + n(i)$$

where h(i) is the complex channel gain and n(i) is the complex AWGN.

At the receiver, assuming perfect synchronization and channel estimation, the received symbols are equalized by a zero-forcing (ZF) equalizer. The equalized symbols obtained by the one-tap ZF equalizer are given by:

$$y(i) = x(i) + \tilde{n}(i)$$

where $\tilde{n}(i) = n(i)/h(i)$ is still complex AWGN noise. For evaluation of the bit-metrics in a soft-demapper, we adopt an approximate scheme suggested in [7]. Then, the bit metrics obtained by soft-demapping are clipped, quantized and finally decoded.

Concerning channel coding, the code parameters are summarized in Table I. In the case of LDPC coding, we have decided to evaluate both the longest and shortest LDPC code from IEEE 802.16e, with the code length (N) of 2304 and 576 bit, respectively. Our selection of those two LDPC codes is driven by a fact [12], that a longer LDPC code performs better error-correction for the same structure of a parity-check matrix (PCM). Therefore, we can expect that all other LDPC codes (in total 17 of them) from IEEE 802.16e have the error correction performance between the two selected codes. We employ a block interleaver in order to improve the performance of RS-CC coding. According to [3], the block interleaver with a depth (ID) of 5 gives near to optimal performance. On the other hand, in the case of LDPC coding, no interleaver is employed. In addition to the basic code-rate of 1/2, we evaluate the performance of channel codes with rate-2/3. Note that in the case of the concatenated RS-CC code, the total code-rate is a little reduced by factors 0.937 and 0.874 for the code-rates of the RS outer codes, RS(255,239) and RS(255,223), respectively. The LDPC code with rate-2/3 is compared to the RS-CC concatenated code with the CC of rate-3/4. Such comparison is performed since the total code-rate of the RS-CC code with the CC-rate-3/4 is closer to the LDPC-rate-2/3 than the RS-CC code with the CC-rate-2/3. In the case of convolutional coding, the rate of 3/4 is obtained by puncturing. On the other hand, in the case of LDPC coding, we use a particular PCM corresponding to rate-2/3 as defined in standard IEEE 802.16e.

Although higher coding rates (3/4 and 5/6) for LDPC coding are supported in the IEEE 802.16e standard, we decided not to consider them in this paper. The reason lies in the fact, that in contrast to code-rate of 1/2 and 2/3, the PCM corresponding to code-rates of 3/4 and 5/6 do not support a row permutation explicitly suggested in the IEEE 802.16e standard. That row permutation eliminates data dependency between adjacent layers of the PCM enabling high-speed layered decoding.

The bit metrics at the inputs of the Viterbi decoder are quantized with 5 soft-bits. This quantization is based on our investigation in previous work [9], as well as an investigation published in [10]. To keep the same complexity of the softdemapper, we adopt 5-soft bit quantization of the input bit metrics for our LDPC decoder as well.

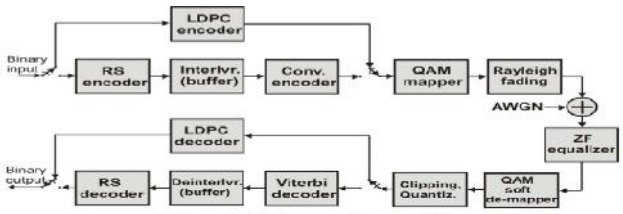

Figure 1. System simulation model

TABLE I CHANNEL CODES PARAMETERS

Channel code	Code parameters
Concatenated code RS CC	RS(255,223)-CC(171,133), ID = 5
	RS(255,223)-CC(171,133), ID = 1
	RS(255,239)-CC(171,133), ID = 5
	RS(255,239)-CC(171,133), ID = 1
LDPC code	N = 2304
	N = 576

3. BER PERFORMANCE EVALUATION

3-A. BER performance optimization of LDPC decoder

The initial bit metrics in both coding schemes are estimated by the soft-demapper and quantized as (1:4). The notation (i:f) denotes the quantization scheme for a total word length of w = i+f bit, where i defines the number of bits for the integer part including the sign bit, and f defines the number of bits for the fractional part. In order to prevent overflow in decoding steps given by equations (3) and (6), that would inevitably lead to poor decoding performance, we introduce the clipping of mn Q

and nAPP messages. If these soft messages are considered as integers, they are clipped symmetrically to) 12(1 −± −w . The BER performance of the LDPC code with N = 2304 bit with three different quantization schemes as well as three different attenuation factors has been investigated by extensive simulations. The simulations are done under 16-QAM over Rayleigh fading channel. The simulation results are shown in Fig.2-3, for the rates of 1/2 and 2/3, respectively. The attenuation factors are determined to be s1 = 0.75, s2=0.8125 and s3 = 0.875, when considering efficient hardware implementation (without using multipliers). As can be seen, in all cases when the word length of the soft information is w = 7 bit, the decoding performance is very poor. The reason is that for these cases, the quantization range is not wide enough resulting in severe saturation produced by the clipping given by equations (4) and (7). An extension of the word length for one additional bit (w = 8 bit) leads to significant performance improvements. In the case of rate-1/2 with s1 = 0.75 and s2 = 0.8125, we did not notice any performance improvement with further extension of word length (for w = 9 bit). Nevertheless, the decoding algorithm with s2 = 0.8125 achieves better performance (about 0.4 dB coding gain at BER=10-6) relative to s1 = 0.75, with a tendency of further improvements when the BER falls under 10-6. In the case of s3 = 0.875 with w = 8 bit, the decoding performance is still poor. A significant improvement can be achieved with w = 9 bit, and even better performance relative to s2 = 0.8125 in the region where the BER falls under 10-6. When considering a target BER=10-6, in the case of rate-1/2, we determine the combination s2 = 0.8125 and w = 8 bit as the optimal choice. A similar analysis can be done in the case of rate-2/3. In this case, we determine the combination s1 = 0.75 and w = 8 bit as the optimal choice.

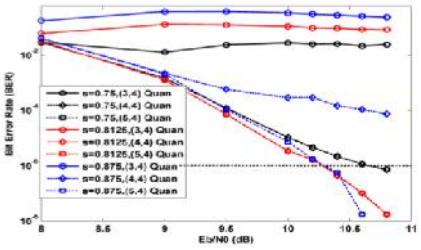

Figure 2. BER performance of the N= 2304 LDPC code, code rate 1/2

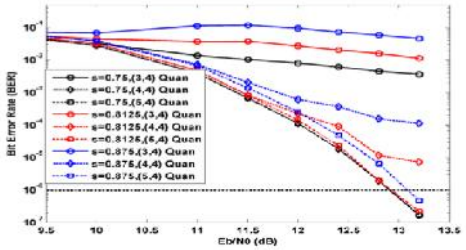

Figure 3. BER performance of the N= 2304 LDPC code, code rate 2/3

3-B. Early Termination strategy in LDPC decoder

In order to detect that a correct codeword is found, an early termination (ET) strategy shall be used. Otherwise, the iterative decoding process will not stop until the maximum number of iterations is reached which causes unnecessary calculations. From a hardware implementation point of view, those calculations lead to decreased decoder throughput and increased power consumption. Therefore, to address this problem, the implementation of an ET strategy is necessary. The common and mathematically exact method of ET is Hc checking. However, in a layered decoder, implementation of Hc checking is inefficient because of high hardware complexity.

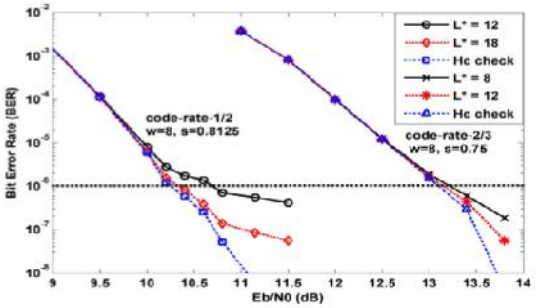

Figure 4. BER performance of N=2304 LDPC code, with the ET strategy

As could be expected, the case L* = 1.5L improves the performance and considerably lowers the error floor relative to L* = L, at the expense of half of an iteration more. However, the average number of iterations is still reduced significantly for medium to high Eb/N0 which leads to an improvement in terms of decoding throughput and power consumption as well.

The performance loss of the ET strategy with L* = 1.5L in comparison to Hc checking is small. In the case of rate-1/2, at a BER=10-6 the loss is about 0.1 dB, whereas in the case of rate2/3, the loss is even smaller, about 0.05 dB.

3-C. BER Comparison between LDPC vs. RS-CC code

Based on the system model given in Fig.1, the BER performance of the channel codes summarized in Table I have been investigated. The MSL algorithm performs with parameters determined as optimal in chapter III-A. The results are shown in Fig.5-6. Summarizing the curves, we draw some conclusions. It can be easily observed that RS outer coding gives a big performance gain in comparison to only CC coding. The bit errors remaining after the inner Viterbi decoder are typically clustered in short bursts, which can be corrected by the outer RS decoder. By using a block interleaver of depth ID = 5,

further coding gain can be achieved, which is quite large (more than 3 dB) especially in the case of rate-3/4 of the CC. Without interleaving, burst errors tend to occur within a single RS codeword, resulting in a tendency to exceed the errorcorrection capability of the RS decoder. The purpose of interleaving is to distribute those burst errors among a number of RS codewords, equal to the interleaving depth (ID).

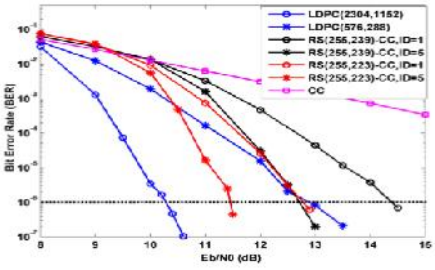

Figure 5 BER performance of RS-CC code and LDPC code, 16-QAM, code-rate-1/2

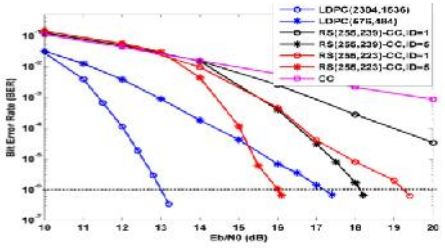

Figure 6 BER performance of RS-CC code and LDPC code, 16-QAM, code-rate-2/3 (LDPC), code-rate-3/4 (CC)

In the case of LDPC coding, a few important observations can be made. The longest LDPC code with N=2304 bits outperforms all considered CC-RS codes, in the range of approximately 1.2 dB (for rate-1/2) to 3 dB (for rate-2/3) relative to the RS(255,223)-CC code, with ID = 5. The shortest LDPC code with N = 576 bit performs a little worse relative to the RS(255,239)-CC code, with ID = 5, for rate-1/2. However, we emphasize that the true code rate of the RS(255,239)-CC is 0.468, causing a data-throughput loss of 6.3% relative to the LDPC of rate-1/2. On the other hand, in the case of rate-2/3, the LDPC code outperforms the RS(255,239)-CC code by about 0.9 dB, but with a data-throughput loss of 5.4% relative to the RS(255,239)-CC code, where the CC is with rate-3/4.

4. DECODER COMPLEXITY COMPARISON

The concatenated and LDPC decoder have been synthesized with an Infineon 40 nm CMOS design kit using the Synopsys Design Compiler. The block deinterleaver (ID = 5) including a depuncturing logic incorporated in the concatenated decoder is implemented in a simple way using 5 dual-port RAMs and an additional control logic. The synthesized cell area, maximum frequency (under worst case conditions) and data throughput are summarized in Table III.

TABLE III SYNTHESIS RESULTS OF DECODERS

	Cell area (mm^2)	Max. clock freq. (MHz)	Max. Throughput (Gbps)	
Viterbi Decoder	0.105	540	0.54	
RS Decoder	0.088		4.05	
Deinterleaver	0.073		1.32	
LDPC decoder, N = 2304 bits	0.79	445	R=1/2	1.013
			R=2/3	1.774
LDPC decoder, N = 576 bits	0.21	445	R=1/2	0.441
			R=2/3	0.787

5. CONCLUSION

In this paper, we have provided a trade-off analysis between concatenated RS-CC and LDPC codes based on a twofold criterion: BER performance over an independent Rayleigh fading channel and decoder complexity for a target data-throughput of 10 Gbps. We have focused on widely used channel codes used in existing communication standards. First, based on simulation results, we have provided an analysis of the relevant parameters of a LDPC decoder focusing on an attenuation factor in the MSL algorithm, the finite word length of the soft information and an early termination strategy. Then, we have shown that even the shortest LDPC code in IEEE 802.16e performs very competitive relative to the RS-CC code in terms of BER performance. All other LDPC codes outperform the RS(255,239)-CC code. On the other hand, in order to achieve a target throughput of 10 Gbps, the LDPC decoder requires significantly more hardware (up to 183 % more gates for N = 2304 bit and rate-1/2) in comparison to the concatenated RS-CC decoder. We have implemented the typical hardware architectures in terms of area and throughput efficiency. Future

work will include an analysis of power consumption as well.

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