# Implementation of Multichannel UART Controller Based on FIFO Technique and FPGA

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*Abstract*— In order to transmit large amount of data over a long distance, serial communications are used. If complex systems are running at different baud rates generated by some special baud rate devices, in this condition common serial ports were unable to meet the requirements. In this case without a unique baud rate controller one cannot implement multi-baud rate communication system. To take care of this issue, in this paper we have planned a Multi-Channel UART controller which depends on FIFO procedures on FPGA. In M-C UART the data received at certain baud rate to the UART and that data can be transmitted to sub controller at the same or different baud rate. In structuring of the computerized circuits FPGA put a significant job and it likewise improves the framework combination, power utilization and unwavering quality.

***Keywords:*** FPGA Spartan-6, UART, COM1

## I. INTRODUCTION

In modern days due to the advancement in technology complex algorithms are easily implemented by modern micro-controllers and processors in order to achieve the expected system performance. In case of the control system the various factors are affected by the results of the system such as bit error rate, baud rate and also synchronization between the subsystems. UART is one of the most used communication methods in the computer system. Essentially, UART is a sequential correspondence framework and with the assistance of this framework we can oversee both parallel just as sequential information move, yet in some of the communication system, serial or a parallel port are used to control the master and slave system. Parallel communication needs multiple bit address bus so it can be used for a minimum distance data transmission. In order to transmit large amount of data over a long distance, serial communications are used. When the complex systems are running on different baud rates with some special baud rate devices, the common serial ports are unable to meet the requirements., The equipment are set to different baud rates such as 57600 bps, 19200 bps, 9600 bps and some other baud rates , while the PC baud rate is set to 115200 bps, in this case without a unique baud rate controller we cannot implement multi-baud rate communication system.

Issue Statement UART three impediments, which impact its proficiency, are recorded beneath

- In a standard UART it has just single channel. Used to connect a single device so when the number of the chip increases on the devices which may cost a lot of space and resource?
- In a flame operation of the microprocessor interrupt request are used to notify the operation. When many interrupt requests occur the processor stuck so the processor efficiency will reduce because number of interrupt request and a few characters are transmitted during each time
- In processor the data bus is 32 bits but some of the cases only one bit of the data is transmitted by the controller to the processor at a time so remaining bits are not used properly.

The over 3 expressed issues are comprehended by utilizing more UART diverts in a solitary chip. So, in this proposed project we are implementing parallel processing data, interrupt control mechanism with the help of MULTICHANNEL UART controller-based FIFO technique and realization is implemented using Verilog HDL on FPGA.

## II. MOTIVATION

Communication in modern complex control systems can be done quickly and effectively. To implement communication when master equipment and slave equipment are set at different Baud Rate so it can also reduce the synchronization error between sub-system.

## III. OBJECTIVES

Correspondence in present day complex control frameworks should be possible rapidly and viably. To execute correspondence when ace hardware and slave gear are set at various Baud Rate so it can likewise lessen the synchronization blunder between sub-framework.

## IV. BLOCK DIAGRAM

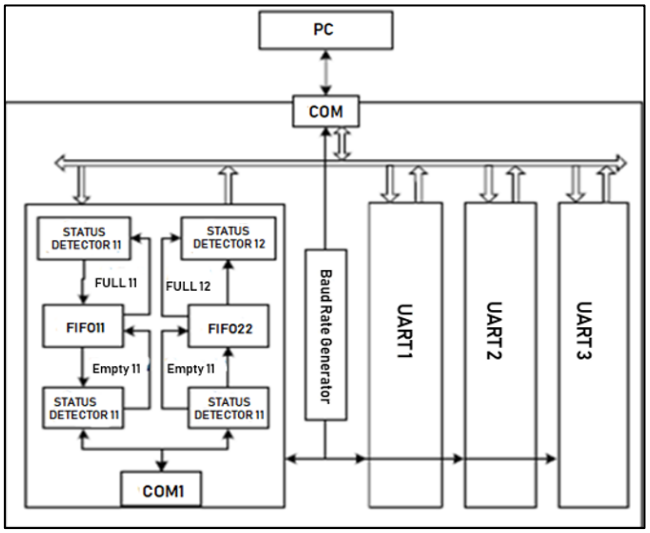


Fig. 1: Block diagram

The UART is essentially a PC equipment gadget used to transmit the information in the middle of parallel just as sequential structure and UART it utilizes TIA and RS-232 AND 485 correspondence principles. In UART the configuration of the information and speed can be

 

configurable so the name is called general and furthermore driver circuit it handles the electric flagging and techniques. UART is a piece of ICs utilized in PC frameworks for sequential interchanges.

UART are fundamentally executed in microcontroller units and it additionally bolsters double UART in a solitary chip and furthermore octal UART underpins eight UART in a solitary chip. In a UART the bytes information is transmitted exclusively in a successive design at the second UART recombines the bits of information as a byte in a UART move register go about as a transformation of sequential and parallel structure. In UART sequential module it is separated into sub module, for example, transmitter module, recipient module and baud rate generator.

## V. DESIGN FLOW

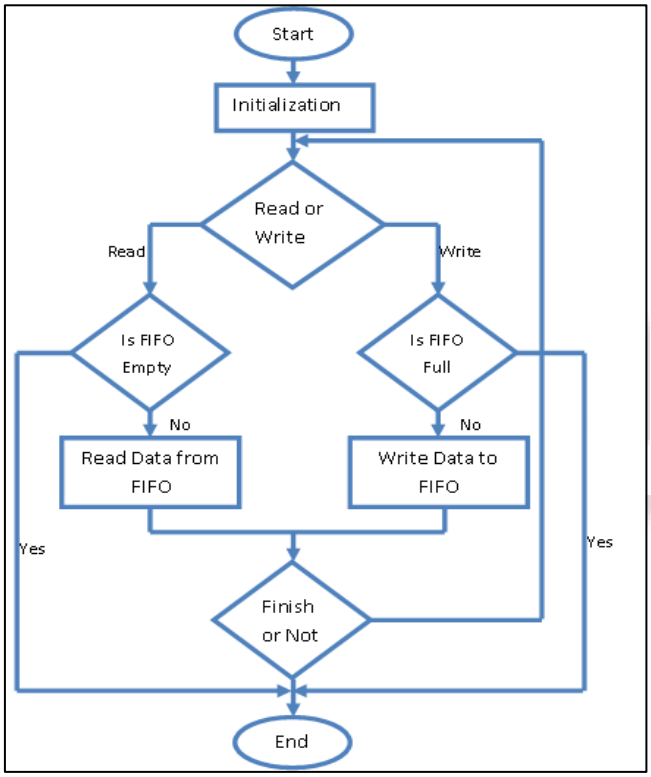


Fig. 2: Design flow

## VI. RESULT

By observing from the figures, we cannot write any more byte into FIFO when the FIFO is full during this condition CS flag is set high to indicate the FIFO full and when the FIFO is empty in this time we cannot read any data from the FIFO and empty is set to high. When FIFO is not full, we can easily write or read the data with the control order.

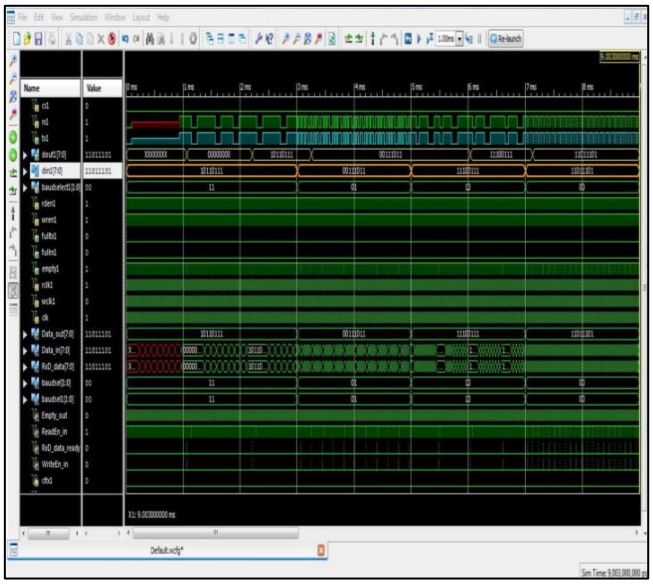

Fig. 3.1: FIFO Read and write

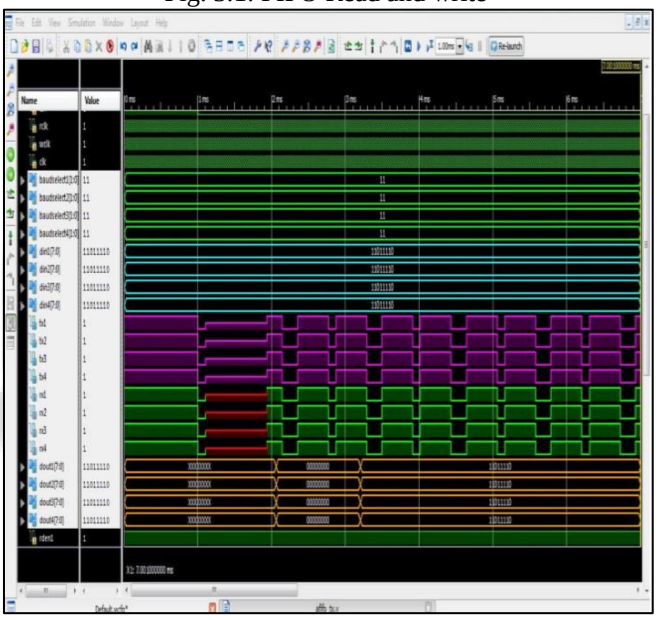

Fig. 3.2: Data Transferred to sub controller with same baud rates

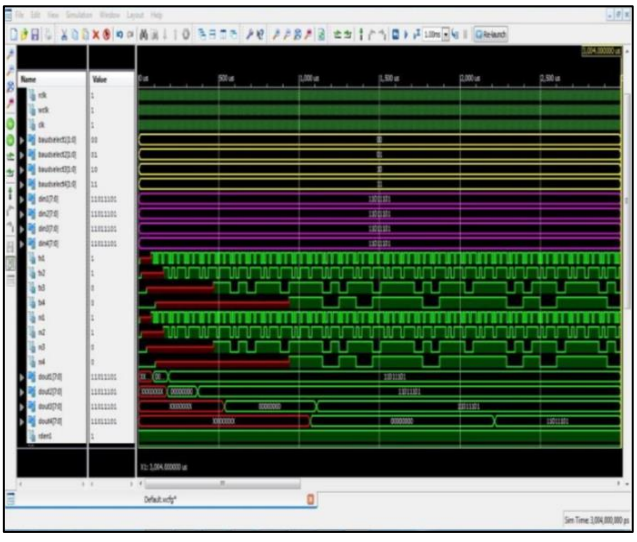

Fig. 3.3: Data Transferred to sub controller with different baud rates

 

## VII. ADVANTAGES

1) Communication in modern complex control systems quickly and effectively.
2) To implement communication when master equipment and slave equipment are set at different Baud Rate.
3) It also can be used to reduce synchronization error between sub-systems in a system with several sub-systems. The controller is reconfigurable and scalable

## VIII. CONCLUSION

It is expected to have better communication between devices with different baud rate. Parallel communication needs multiple bit address bus so it can be used for a minimum distance data transmission. In order to transmit large amount of data over a long distance, serial communications are used. When the complex systems are running on different baud rates with some special baud rate devices, the common serial ports are unable to meet the requirements.

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