FPGA based implementation of SDR transceiver

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Abstract:
Field Programmable Gate Array (FPGA) based transceiver is purely a new kind of digital implementation of transceiver in Software Defined Radio (SDR) platform. This replaces a multiple platform based system with a single platform. It guarantees reliable, reconfigurable, handy transmitter and receiver. A high-level programming language is used to simulate and implement system in real time.

Index Terms **- Field Programmable Gate Array (FPGA), Software Defined Radio (SDR).**

I.INTRODUCTION

For a conventional discrete component-based design of transceiver, it is not possible to vary the functionality of the system beyond certain range of specification. But a SDR based on FPGA enhances the capability of the platform so as to design a system with re-configurability and flexibility. It can flexibly alter the radio waves by changing software and without changing SDR platform. SDR can be implemented in different platform. Here, SDR based telecommunication operation is realized in FPGA, using high level programming language. The main application of digital transceiver lies at the test facility of newly developed flight vehicle. A newly developed flight vehicle needs testing. Termination of flight vehicle is mandatory if the high speed vehicle deviates from its preset trajectory due to unpredictable failures of onboard system. FPGA implementation of digital transceiver in SDR platform System is used for termination of high speed flight vehicle under test. Hence at test facility, this system is utilized to secure property and human life. In such cases, specific commands are transmitted from transmitter for termination of test vehicle. The command transmitted is received and decoded by onboard command reception system at flight vehicle and the commanded operation is done accordingly.

II.SYSTEM MODEL

SDR Based Transmitter Algorithm: SDR based transmitter include command code generation, encoding, digital modulation, analog modulation and digital up conversion. The command codes are inputted from personal computer. The generated commands are a frame of N binary bits. The whole frame is encoded with Manchester encoding scheme and total number of bits in a frame becomes double, i.e., 2N. This Manchester encoded binary data waveform modulates a carrier signal using binary frequency shift keying (BFSK) modulation scheme. In this scheme, sinusoidal signal with higher frequency and lower frequency are generated for bit 1 and 0, respectively. This BFSK modulation is done in very low frequency, i.e., in very-low frequency band. This signal is finally up-converted to medium frequency band using frequency modulation (FM) scheme. The basic principle behind FM is to vary the carrier frequency in proportion to the modulating signal. FM modulated signal is the output of command code generator. This signal undergoes digital up conversion (DUC). To improve the sampling frequency of baseband signal interpolation is used. The primary reason to interpolate is to increase the sampling rate at the output of one system, so that another system operating at a higher sampling rate can operate the signal.

SDR Based Receiver Algorithm: In the receiving side, the received signal is down converted using digital down conversion. FM signal can be demodulated by applying the signal to the All-Digital Phase Locked Loop (ADPLL).
FM demodulated signal is given to BFSK demodulation block. Finally Manchester decoding is done. Code is received & displayed on PC.

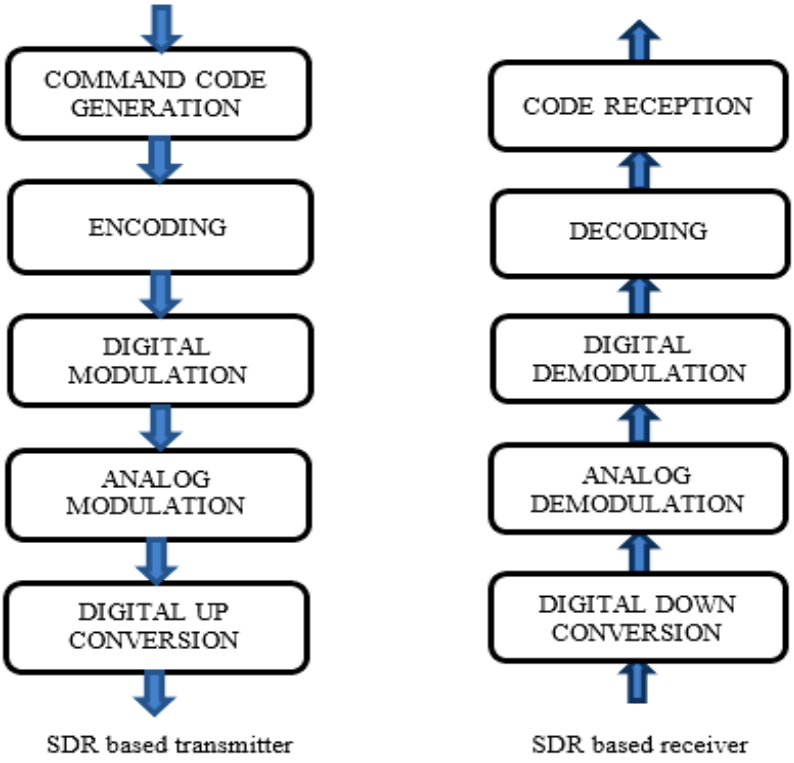

Figure. 1 SDR based transmitter and receiver

III.PROPOSED SYSTEM

The system is implemented in FPGA. The entire system needs different frequencies for baseband data rate, as sampling frequency for BFSK modulation, as sampling frequency for FM modulation and for CIC interpolation module. The Spartan 3 FPGA board has global clock 30MHz. By using DCM in FPGA and clock generation module, required clocks are generated.

Digital Clock Manager (DCM): Spartan 3 has internal clock frequency of 30MHz. The 100MHz clock is generated from 30MHz clock using digital clock manager. In Xilinx clocking wizard general setup, input 30MHz as input clock frequency and input 100MHz as output clock frequency. All the remaining clocks are generated using clock generation sub module. Initially set count and clock as zero. Then increment the count. Select a value for the count in such a way that input clock period multiplied by that value should give required clock period. When the count equals selected value, take negation of clock and set count equal to zero. Then repeat the steps.

Coding Principles of Manchester Code: Manchester code is mainly used in digital systems. It is used to represent the binary values 0 and 1. It represents the binary values by a transition. The transition occurs at midbit, with low to high transition is used to represent a logic zero, and a high to low represent a logic one. A pattern of consecutive ones or zeros result in a transition on the cell boundary. When the data pattern alternates between one and zero, there is no transition at the cell boundary. Manchester code has no DC component, so it can be transformer coupled. The functions of the encoder section include a microprocessor interface, parallel to serial conversion, frame generation, and Manchester encoding. This circuitry does not require a high-frequency clock. The frame format used is similar to that of a UART.

IV.BFSK Modulation

Simulink model for the BFSK modulator is shown in Fig. 2The selected BFSK mark frequency is 50 KHz and space frequency is 10 KHz. By using a switch, if the Manchester encoded output is greater than 0, select constant for BFSK mark frequency and if it is zero, select constant for BFSK space frequency. It is given to the adder based on the output of Manchester encoder. Adder and memory together work as a phase accumulator. Cosine of the phase gives the modulated output.

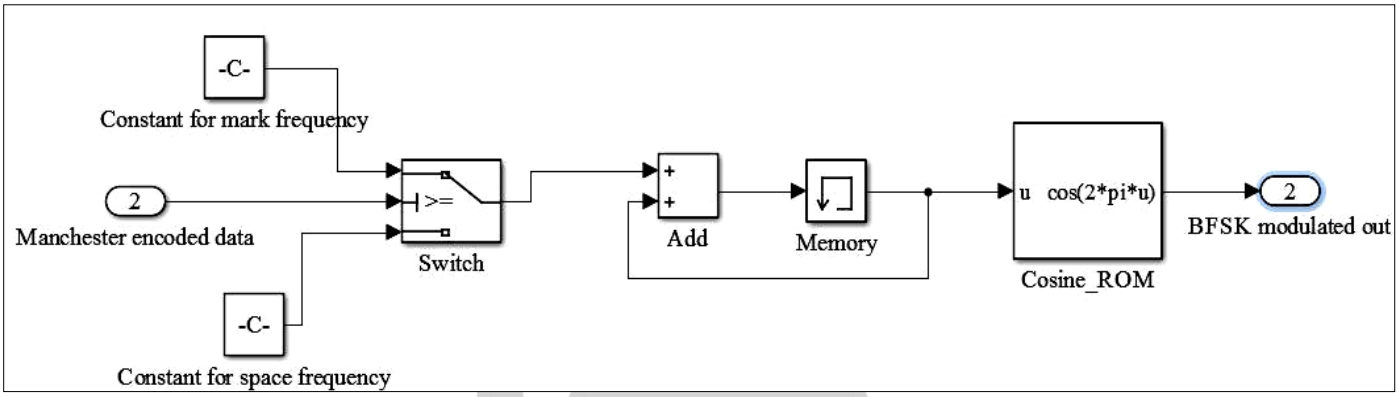

Figure. 2 BFSK modulation

Block Memory Generator:

Block memory generator is used to perform both BFSK and FM modulation. Xilinx provides a flexible Block Memory Generator core to create memories running up to 450 MHz. The Block Memory Generator IP core creates optimized block memories for Xilinx FPGAs. Block memory generator is selected from FPGA features and design. Component name is given as sine_table.

Memory Types: The Block Memory Generator core generates five types of memories: Single-port RAM, Simple Dualport RAM, True Dual-port RAM, Single-port ROM, and Dual-port ROM. Here we need single port ROM.
Selectable Width and Depth: The Block Memory Generator core generates memories with 1 to 4608 bits width, and with depths of two or more words. Here we need to select read width in memory size as 10 bits and read depth in memory size as 32. The data that should be stored in ROM should store as .coe file in the ip core directive of FPGA. In the next step load the .coe file then click finish.

Frequency Modulation:

Simulink model for the combined Manchester encoder and FM modulator is shown in Fig. 3. The selected FM deviation is 250 KHz. The output from BFSK modulator is multiplied with a gain K at a sampling rate of 10MHz. A constant for FM deviation equal to 250 KHz is added with gain block output and is given to phase accumulator. Adder and memory together work as a phase accumulator. Cosine of the phase gives the modulated output.

V.CONCLUSION

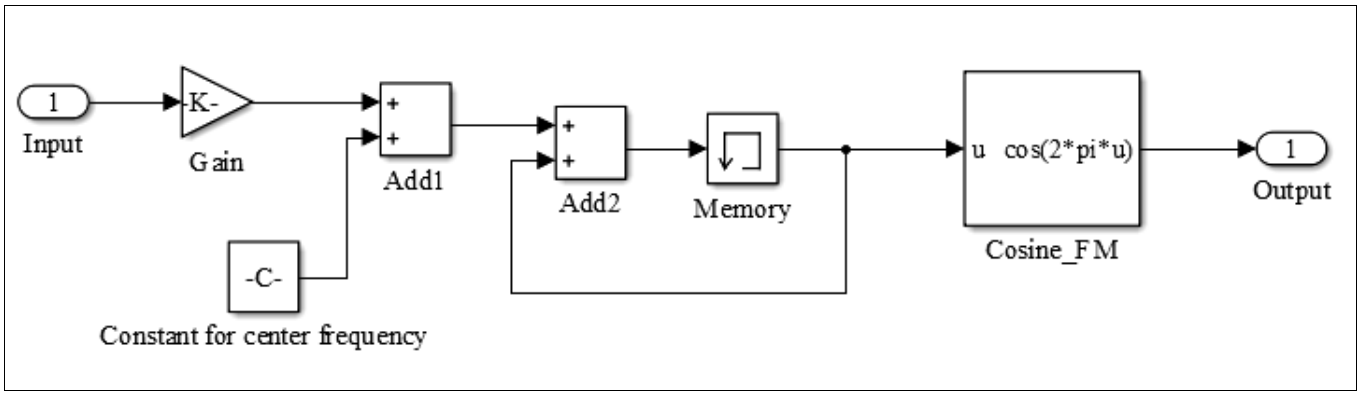

Figure. 3 Frequency modulator

Proposed SDR-based digital transceiver system can be implemented using Xilinx FPGA, gives a very highly flexible platform for complex algorithms for digital transceiver system designing. The system has been designed using Xilinx software. It provides a very reliable and fast communication. Suitable algorithms for signal generation, encoding, and baseband, and pass band modulation, DUC, DDC, demodulation and decoding of design have been chosen and implemented to ensure optimized uses of hardware.

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