Advanced Software Defined Radios for Wireless Communication with Improved Power Efficiency

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Abstract. Radio is one of the most common things that people use around the world. Marconi developed it in 1895 and since then there is no stop in its development, some of the domains like the cognitive radio and Software defined radio have seen great advancements in communication. In the following paper, we will explore the software defined radio and various techniques to implement the radio. When we talk about the Software defined radio every aspect of its operation is performed by controlling software SDR transmitter and Receiver which are used. In this paper, we will focus on the discussion to examine the reconfigurability and low power trade-offs. We will be building dedicated functional modules providing high performance at a high cost (Velcro approach explained below), versus parameterizable function blocks used in FPGA-based system development, and lastly dynamic partial reconfiguration which is the ability to reconfigured a portion of the FPGA while still remaining in operation.

Keywords: Low power consumption, software defined radio, convolutional encoder, dynamic and partial reconfiguration, power gating.

1 Introduction

Software-defined radio (SDR) has revolutionized the total radio system as it has its application over a variety of systems like the communication, data acquisition, and signal processing. It is considered as an emerging technology for processing radio signals by means of software Techniques. The new mobile applications or the mobile devices uses a lot of radio standards than ever before, so to meet up the demands the radio system should be upgraded since the software techniques are considered as solutions to quickly design flexible mobile applications. Such an SDR is also called as the ITS (information transfer system) that combines the technology of the mobile and the radio to make it more efficient and flexible. With an excellent future in wireless communication, there'll be an excellent demand of good instrumentation that may operate underneath many communication situations. Software Defined radio (SDR) is one in every of the technique which may fulfill the increasing demands with associate ease. SDR once employed in a communication system is nothing, however, a system wherever a number of its perform blocks square measure enforced exploitation versatile software package routines instead of some hardware assembled thereto thanks to that multiple operations are often platform freelance and therefore the potency and therefore the would like of significant hardware is additionally reduced by the system. The SDR adapts to the condition and changes consequently to suit the strain of the condition by ever-changing the operation performed. This idea is incredibly fascinating, exploitation reconfigurable computing, it's been undoable for the instant as a result of its tight power budget and its high demand on computation capability.
When such a tool is employed for industrial purpose then the ability allowed for baseband signal process ought to be not up to many hundred mW. Reconfigurability required by the execution core of varied wireless protocols tends to extend the full power consumption of the hardware thus the coming up with the digital baseband process of such terribly an especially versatile system could be a very difficult task since there's solely a restricted battery on the hardware of the wireless system gift to be employed by the system. Thus it's terribly crucial to style SDR.
To implement software Defined radios, varied technologies will be used, like the applying specific computer circuit (ASIC), the digital signal processor (DSP), the sector programmable gate array (FPGA), and therefore the general purpose processor (GPP). The GPP offers the upper flexibility, however, has very cheap performance. However, the ASIC is that the least versatile one, however, has the very best performance. ASIC is em-

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ployed to attenuate power consumption and to maximize performance. The FPGA provides the simplest reconfigurable resolution for prime speed signal process modules that square measure extremely parallel.

In software Defined radio baseband, the GPP, DSP and FPGA square measure usually used for baseband process and therefore the ASIC will be solely used for a few common specific modules like the upconverters and/or downconverters. As indicated on top of, the FPGA provides the simplest balance between performance, low power consumption, and short style cycle. Besides, the new Xilinx FPGA series provides a dynamic and partial reconfiguration practicality that is that the ability to dynamically modify a neighborhood region of logic by downloading partial reconfiguration files whereas the remaining logic continues to control while not an interruption. During this article, we tend to propose to match and analyze 3 hardware implementation strategies to style SDR instrumentality. The primary methodology is that the Velcro approach that is that the classical approach to implementing the various radio standards and modes configuration within instrumentality. This methodology uses a straightforward switch to execute the used mode. The duplication of every chain becomes unfeasible from a technical and economical purpose of read and therefore the crying would like of recent methodology to style terminal reflects that. On the contrary, within the pioneering add [3, 4], authors gift a second style approach, named Parameterization. This approach aims SDR instrumentality wherever every operation will be modified simply by a straightforward parameter adjustment and it will be extended to lower design level. Palicot and al [5] propose a really attention-grabbing technique supported the graph theory for best determination of common functions and best parameters.

More recently, Xilinx introduces a 3rd style approach referred to as FPGA Dynamic and Partial Reconfiguration (DPR) that has been wide studied in academe [9]. The DPR provides the modification of some of the device whereas the remainder remains unchanged and active. Its outstanding blessings like the rise of the system performance, the flexibility to vary hardware, hardware sharing, low power consumption, and really little reconfiguration time. During this article, we have a tendency to study performance, reconfigurability, and power consumption of the 3 style approaches. Within the literature, there aren't several papers revealed, according to the simplest of our information, that regarding the impact of the hardware style technique on power consumption within the context of SDR instrumentality style. The analysis is finished employing a classical convolutional encoder block. This is often an easy example, however, the conception will simply be extended to produce a lot of helpful and complicated signal process practicality. During this work, we have a tendency to fail to absorb through numerous power minimization techniques like clock gating, dynamic voltage and frequency scaling, and multiple voltage islands. Within the remainder of this paper, Section a pair of explains the specificities of a convolutional channel encoder. Section three presents the various style approaches to implementing the channel decoder block victimization Velcro, parameterization, and DPR techniques. The experimental results square measure according to in Section four. Section five concludes the paper and discusses some future directions.

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2 System view:

FPGA technology provides the signal-processing engineer with the ability to construct a custom data path that is tailored to the application at hand. FPGA reconfigurable DSP system is shown in Fig.1.

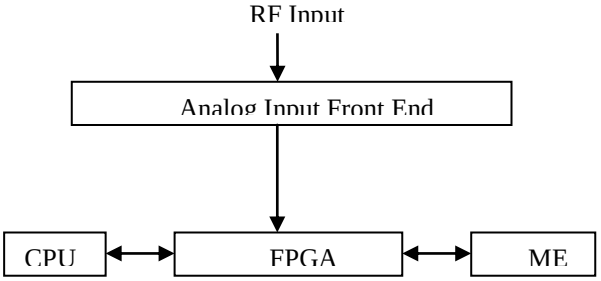

Fig.1. Reconfigurable DSP System

3 Design parameters

Many run-time reconfigurable systems square measure designed in AN ad-hoc manner. During the planning method, it's usually unclear however the final implementation can perform. We have a tendency to propose a structured style approach that identifies style parameters and maps these onto the reconfigurable device. Within the following, we have a tendency to contemplate 3 implementation attributes: performance, space, and storage. First, we have a tendency to establish parameters of a reconfigurable module: – space demand A – interval tp for one packet or data point – Reconfiguration time tr – Configuration storage size Ψ – the amount of process steps s

within the formula – the number of correspondence p within the implementation we can square measure able to} conjointly establish parameters of the appliance that employs a reconfigurable module:

– needed knowledge outturn φapp

– The amount of packets or things of knowledge n that are processed between reconfigurations

The reconfigurable device is defined by the subsequent parameters:

– The obtainable space A_{max}

– The info outturn of the configuration interface φ_{config}

– The configuration size per resource or unit of space Θ.

4 Convolutional encoder

Convolutional codes were introduced by Peter Elias [6] in 1955. They're the wide used channel codes in sensible communication systems. Convolutionally secret writing the information is achieved employing a register and associated combinatorial logic that's typically within the sort of cascaded exclusive-or gates. The encoded bits rely upon this k input bits and on past input bits. They're delineated by 3 integers, (n, k, K), wherever the magnitude relation k/n is termed the code rate and K could be a parameter presents the constraint length; it represents a number of k stages within the secret writing register. The constraint length K determines the aptitude and therefore the quality of the code. Many coding algorithms are planned within the literature, however, the foremost well-known is perhaps Viterbi formula [7]. Like the bulk of codes, convolutional codes generally use binary symbols. Figure one illustrates an easy (7; 5) binary convolutional encoder of constraint length K = three.

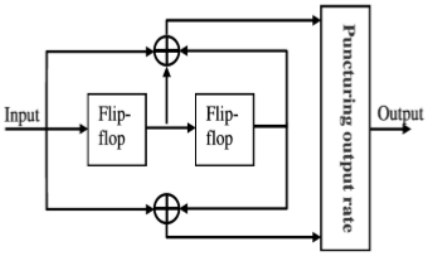

Fig.2. Example of convolutional encoder with r=1/2 and K=3 [14]

The positional notation numbers seven and five represent the code generator polynomials, that browse in binary (111_2 and 101_2). It corresponds to the register connections to the severally higher and lower modulo-two adders. The selection of the connections between the adders and register offers rise to the characteristics of the code. At every input bit time, to a small degree is shifted into the left stage and therefore the bits within the register square measure shifted one position to the correct. The output switch presents the sample of the output of every modulo-2 adder, forming the code image combine related to the current input bit. The sampling is continual for every inputted bit. So as to estimate and analyze the impact of the implantation technique on power consumption, we have a tendency to think about here some samples of convolutional encoder utilized by the world System for Mobile communications (GSM), the Universal Mobile telecom equipment (UMTS) and 802.11g wireless standards. Table one presents the polynomials generator utilized by higher than standards.

Table 1. Generators Polynomial Used

Conv. Coding	Rate	Generators Polynomials
GSM TCH/FH TCH/HE	1/2	G0 = 31 G1 = 33
	1/3	G4 = 155 G5 = 123 G6 = 137
UMTS BCH, PCH TCH/HE	1/2	G0 = 561 G1 = 753
	1/3	G0 = 557 G1 = 663 G2 = 711
802.11G (OFDM Mode)	1/2	G0 = 133 G1 = 171

We can implement our channel encoder employing a synchronous model, during which all blocks are assumed to possess finished computation once a clock edge arrives. During this paper, we are going to use a globally

asynchronous domestically synchronous (GALS) model. During this model synchronous practical blocks with domestically generated clocks are used with asynchronous connections between them.
Therefore, we tend to retain the benefits of synchronous circuits, and that we will exploit the benefits of asynchronous routing at the identical time. The designed system consists of blocks which might be on an individual basis optimized and therefore the temporal arrangement of 1 block doesn't have an effect on the opposite blocks. The channel encoder may work on totally different standards like GSM, UMTS and in several modes as an example GSM-TCH, UMTS-BCH. We tend to implement the channel encoder victimization 3 approaches: Velcro, Parameterization, and DPR.

4. Design approaches

The main objective of this work is to review the impact of style approaches within the performance of the system. We tend to propose 3 totally different implementation strategies that are Velcro, Parameterization, and DPR.

4.1 Velcro approach

In Velcro approach [12], every customary is optimized and might be enforced as A freelance process unit (PU). The interchange between this PEs will be created by employing an electronic device. The shift from one customary to a different will be done throughout one clock cycle. However, all standards should be enforced on thechip which might increase the world power consumption of the look.

4.2 Parameterization approach

The parameterization approach [12] relies on victimization parameters to modify from one customary to a different. During this approach standards share resources. To commute between totally different standards, we must always solely modify the polynomial generator parameters as an example. This approach consists within the reusing of identical style to perform totally different standards. To style parameterization design the worst case should be enforced. This approach reduces the world utilization however it becomes additional complicated if the quality of parameters is hyperbolic. Moreover, the look typically needs over one cycle clock to commute between 2 standards.

4.3 DPR approach

Dynamic partial reconfiguration is the ability to vary the configuration of a part of AN FPGA device whereas alternative processes continue within the remainder of the device [10]. Xilinx suggests in 2 basic techniques of DPR on one FPGA: the module-based and therefore the difference-based partial reconfiguration. The difference-based will be used once a little modification is created to the look. It's particularly helpful just in case of adjusting look-up table (LUT) equations or memory blocks content. The generated partial bit stream contains solely info concerning variations between this style and therefore the new content of AN FPGA. Shift the configuration of a module from one implementation to a different is extremely fast, because the bit stream variations will be extraordinarily tiny. The module based uses standard style ideas to reconfigure blocks of logic. The distinct parts of the look to be reconfigured arecalled reconfigurable modules, as a result of specific properties and specific layout criteria should be met with relation to a reconfigurable module, any FPGA style desiring to use partial reconfiguration should be planned. A partially reconfigurable style generally includes a locality for static modules and one or additional partial reconfigurable modules (RM). The static modules contain logic that may stay constant throughout partial reconfiguration. Partial reconfiguration module is that the style module which will be swapped within the device on the time period multiple modules will be outlined for a selected FPGA region. Within the early Virtex family devices like Virtex-II and Virtex-II professional devices, we tend to should partly reconfigure whole columns. Recently, in Virtex -4/5/6 devices, the partially reconfigurable region (PRR) is rectangular of arbitrary size and will be situated anyplace with no overlapping. Throughout Partial reconfiguration method, the routing signals used for inter-modules communication ought to be unchanged once the module is reconfigured. This fastened routing bridge of communication is achieved by victimization bus macros.
Bus macros are onerous macros that are found at the string of boundaries separating dynamic and static regions. To load the partial bit stream, designer ought to use an interior configuration access port (ICAP). The Virtex-II series are the primary architectures that support ICAP that may be a set of the Select MAP interface having fewer signals. The ICAP solely deals with partial configurations and ought not to support totally different configuration modes. It provides AN eight input/output bits knowledge bus.

Whereas with the Virtex-4 and Virtex-5 series, the ICAP interface has been updated with thirty-two input/output bits knowledge bus to extend its information measure and speed up the reconfiguration time. The intuitive edges of victimization DPR are: the development of FPGA space potency [11], the augmentation of architectures flexibility, the decrease of power consumption AND smaller FPGAs will be want to run an application as a result of to commute between totally different standards, we will simply load the partial reconfiguration bitstream. However, the implementation method for DPR continues to be complicated and tedious, and therefore the designer ought to have an intensive understanding of the underlying device and style methodology. In our case study, the convolutional encoder design consists of a static module containing primitive operators as XOR gates and shift registers, and a dynamic module. The partially reconfigurable module will be seen as an affiliation matrix with restricted property wherever every matrix part admires the affiliation or not between registers outputs and XOR gates inputs.

5. Performance

All the on top of style approaches are tested with similar standardized tests that area unit wont to measure and to verify the convolutional channel encoder associated with totally different standards. Table 2 shows space prices of the 3 style techniques at the frequency of 360megacycle per second.

Table 2. On-chip area costs using different design approaches

	Velcro	Parameterization	DPR
LUTs	77	57	38
Flip Flop	140	78	51
I/O	9/3	14/3	5/3
Frequency Max (MHZ)	359.409	360.021	360.888

The Dynamic and Partial Reconfiguration technique reduce space by decreasing the quantity of style parameters and input/output ports. We are able to conclude that the DPR approach ends up in quite forty-ninth average reductions in space prices for Virtex-5. The comparison between the 3 on top of architectures in terms of hardware resource shows that the partially reconfigurable approach has the best process rate. In fact, the Velcro technique needs additional space than the parameterization and dynamic and partial reconfigurable architectures.

Table 3.Total power consumption estimation for different design approaches

	Leakage Power (w)	Dynamic Power (w)	Total power (w)
Velcro	0.053	1.288	1.341
Parameter-ization	0.041	1.288	1.329
DPR	0.027	1.286	1.313

In table 3, we tend to provide the full power consumption estimation for the on top of 3 style approaches. To urge associate out there an estimation of static and dynamic power consumption of the used FPGA device, we tend to use Xilinx Power calculator (XPE) tool. The approach employed by the Xilinx Power calculator consists of providing info as well as the quantity of LUTs, flip-flops, DCM, DSP, the common switch at intervals the FPGA, and also the clock frequency for working out the ability consumed by the FPGA at a given temperature [8]. The XPE tool relies on associate stand out a computer program. The advantage of those tools is that results area unit obtained in no time. Moreover, the results area unit correct for dynamic and static power consumption.

Table 4. Design time

	Design Time
Velcro	1 day
Parameterization	1 day
DPR	2 days

We note that DPR design has the best style time. This is often in the main because of the complexness of the look flow used for the DPR technique. Indeed, compared to a static system, the planning of a partly reconfigurable system needs extra design steps, like partitioning the appliance into static and dynamic modules, adding the

ICAP, develop a C code to manage the partial reconfiguration bitstreams, etc. the planned properties of the 3 projected design ways area unit ended in table five resting on four aspects: process rate (area), performance, power consumption and configuration time overhead.

Table 5. Properties of design approaches

	Velcro	Parameterization	DPR
Area	Low	Adequate	High
Performance	Adequate	Adequate	Adequate
Power	Low	Adequate	High
Conf-overhead	High	Adequate	low

We can see in table 5 that, the Velcro style approach has very cheap configuration time overhead as a result of the switch time between totally different normal is holding only 1 clock amount. However, its highest space waste makes the system power inefficient. Parameterization approach ensured less space waste than Velcro consistent with these hooked up parameters for reprogramming between totally different normal. If we tend to use a Virtex-II FPGA, the ICAP can operate at fifty megacycles per second and eight bits information dimension port, the reconfiguration time is extremely multiplied.

Techniques for reducing switching activity

Lowering the switching activity is a very promising way of decreasing the power consumption. There are numerous researches on this issue. In this section, we introduce system level approaches for reducing the switching activity. System level switching activity reduction can be categorized as follows: • Turn off unused HW modules.

There are two main shutting down strategies: clock gating and power gating.

1. Power gating is mainly used for reducing leakage power.

2. The best-known technique for reducing the switching activity is clock gating.

	Clock Gating	Power Gating
Hardware support	Easy	Difficult
Overhead (power & area)	Small	Large
Overhead (delay)	Small	Large
Energy efficiency	Moderate	Large

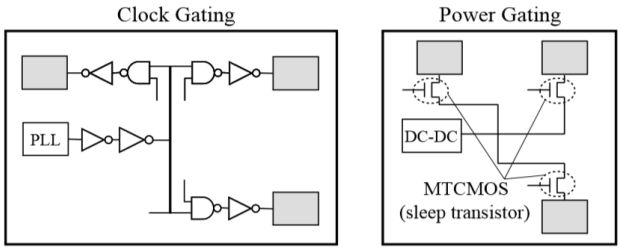

Fig 3. Clock gating and power gating comparison

Although lowering the supply voltage is the most effective way of reducing the energy consumption of the chip, this causes an increase of circuit delay, τ, which determines the maximum clock frequency of synchronous circuits. The delay τ of a CMOS circuit can be approximately formulated as

$$\tau \propto \frac{V_{DD}}{(V_{DD} - V_{th})^2} \cong \frac{1}{V_{DD}}$$

Where Vth is the threshold voltage of CMOS transistors used in the circuit. Basically, we have the following three ways for lowering the operating voltage without sacrificing the performance of the system. 1. Parallelize tasks so that the performance does not degrade even in a low voltage operation. The approach is refered as static voltage scaling. 2.

Lower the clock frequency and operating voltage when the maximum performance is not needed. The approach is referred as dynamic voltage scaling.

The conditional clock for the power-down mode must be designed with all the caveats applied to any conditional clock—the conditioning must meet skew and edge slope requirements for the clocking system. Static or quasi-static memory elements must be used in the powered-down section for any state that must be preserved during power-down.

Power consumption in clocks due to:

- Clock drivers
- Long interconnections
- Large clock loads –all clocked elements (latches, FF's) are driven

- Different components dominate
  - Depending on type of clock network used
  - Ex. Grid –huge pre-drivers & wire cap. Drown out load cap.

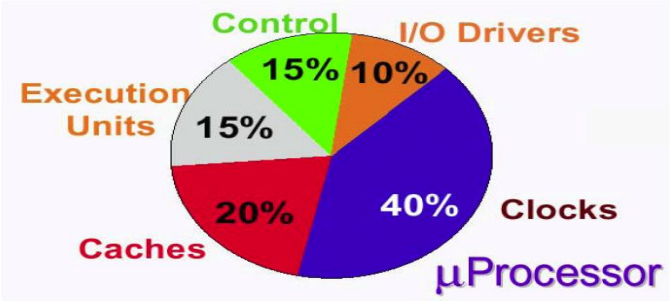

Fig 4. Clocks: Power-Hungry

Low Power Clocking Techniques: Gated clocks

- Prevent switching in areas of the chip not being used
- Easier in static designs

- Edge-triggered flops
- Reduced load on clock for each latch/flop as well as eliminated spurious power-consuming transitions during flow-through of latches

Clock Distribution Metric: Area

- Clock networks consume silicon area (clock drivers, PLL, etc.) and routing area
- Routing area is most vital
- Top-level metals are used to reduce RC delays
  - These levels are precious resources (unscaled)
  - Power routing, clock routing, key global signals
- By minimizing area used, we also reduce wiring capacitance & power

6. Results and discussion

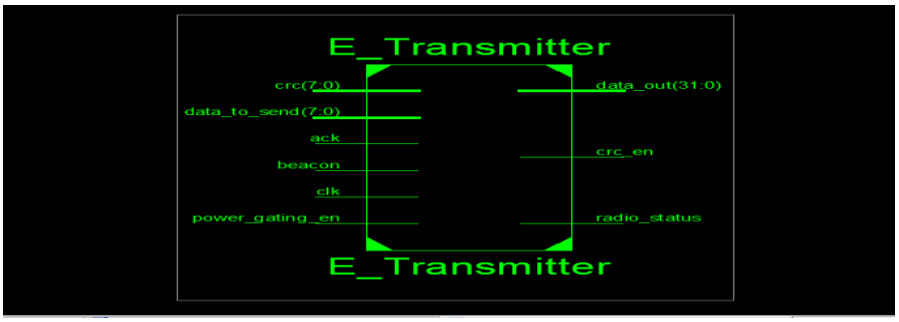

Fig 5. Transmitter with power gating

The whole system consists of transmitter and receiver, the transmitter with power gating and the beacon is shown in the fig 5.Power gating is used to improve power efficiency in the communication system.

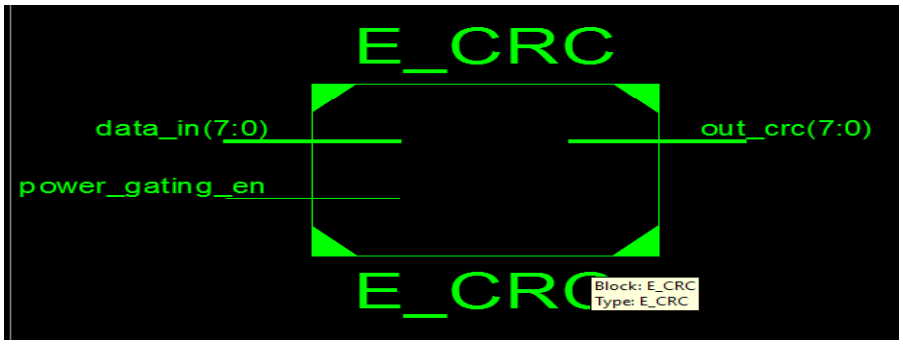

Fig 6. CRC block in transmitter

In a communication system, the received data is may be or may not be error free. During travelling from the transmitter to receiver many sources are there to alter the contents of data. To check and correct the error CRC block is introduced.

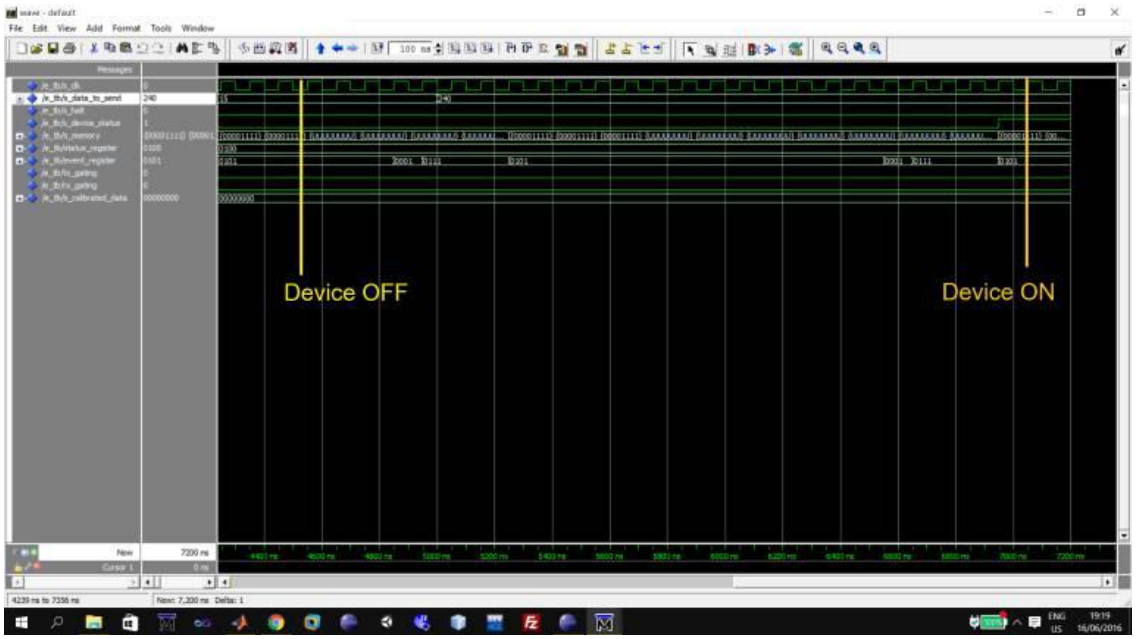

Fig 7. Simulation results of transmitter

Receiver initiated communication is required to save the power. At the receiving end if and only if receiver requires data from transmitter then only it sends otherwise not. In the simulation results it is shown that depending upon device (means the receiver is ON or OFF) status, transmitter gets the acknowledgment and accordingly it acts.

7 Conclusion

In this paper, we analyzed three techniques namely Velcro, Parameterization and DPR. As the paper suggests that DPR performs best in terms of all the parameters mentions like delay, power, and total power consumption. The DPR performances can be amplified which is the field of research, the performance consideration of Velcro and Parameterization are kept in mind while designing the final system. The power of DPR can be optimized using different communication system likewise the transmitter and receiver can be amplified.

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