Curriculum Vitae

1. Name: **Dr. Dilip. D. Chaudhary**

2. Designation: Vice-Principal and HoD E&TC dept., SIT Lonavala

Email: dchaudhary.sit@sinhgad.edu ,
Mobile: 9372810161, 9420305869

5. Date of Birth: 20/02/1964

6. Address: C-304, Grande View- 7, Ambegaon, Pune.411046.7. Research Interests: Wireless sensor Networks, Control and Automation.

Educational Details:

- Ph.D. (Instrumentation Engineering), From SRTMU Nanded, April 2016.
- M.E. (Digital Tech. & Instru.) from DAV, Indore, First class with distinction, April 1991.
- B.E. (Electronics and Power) from Govt. College of Engineering, Amravati, First class June 1985.
- H.S.C. (Technical) from Govt. Technical College, Amravati. First class, April 1981.

Experience: (36+ years)

- 1985 to 1992:- Lecturer in Electronics Dept. at SSVPS College Engineering, Dhule, MS .India
- 1992 to 1993:- In-Charge Principal at Gangamai college of engineering, Nagaon, Dhule, MS India
- 1993 to 2006:- Assistant **Professor** in Electronics Dept. at SSVPS College Engineering, Dhule, MS, India.
- 2006 **till date**: Working as a **Professor** in E/TC Dept., Sinhgad Institute of Technology, Lonavala, India.

Responsibilities:

Working as a Vice-Principal and Head of E&TC Dept. at SIT Lonavala.

Research publications:

- International Journals: 14, National Journal: 02, International Conference: 08, National Conference: 03
- Google Citation: **360**, h-index: **06**, i10 index: **05**. (**As on 22/05/2022**)
- One Australian Patent No. 202111026315 dated 14th June 2021, Granted on 'A METHOD FOR EMPIRICAL RISK ASSESSMENT OF BRAIN DISORDER USING NEURAL NETWORK DIAGNOSTIC SYSTEM Name of inventor(s):Upreti Kamal, Raut Ranjana, Dinkar Raut, Abhishek Dinkar, Gupta Stuti, Agrawal Chaitanya, Bansal Mukesh, Chaudhary Dilip, and Suthar Naresh Kumar.
- Published **Text book** on "Electronic Product Design' for B.E. (E&TC) as per SPPU syllabus.
- Published **Text book** on "Electronic Product Design' for T.E. (Elex. Engg) as per Mumbai Univ. syllabus.
- Worked as a **Research Fellow** at Aalborg University, Denmark under **European Union Scholarship** Program from September 1, 2010 to May 31, 2011.

Professional Membership:

• IEEE (90659696), IETE (F189075), ISTE (23509), IE (M115453), ISA (33188566),

Achievements and Awards:

- Worked as a Ph.D. Thesis reviewer for Perugia University, Italy.
- Worked as a **SPOC for NPTEL** for more than five years.
- Working as a Nodal Coordinator for **V-Lab**, Coordinator for **PMKVY** at the Institute.
- Working as a Subject Chairman for final year subjects AVE, TVE and EPD at SPPU Pune.
- Worked as **convener** for the First International conference 'GISFI'. At SIT Lonavala.
- Worked as an **organizing committee** member and **Reviewer** for International conferences and Journal.
- Worked as a **Staff Selection Committee** member at University level.
- Worked as **Subject Chairman** and **Resource person** in FDP at Pune University.
- Delivered **key note speech** at International conferences, Motivational Lectures at various Institutes.
- Worked as a Key member for NBA and NAAC and working as a IQAC coordinator at the Institute.
- Started professional Clubs like IE, ISTE, IEEE, TG scheme, foreign language courses at the Institute.

Date: - 22/ 05/ 2022 Place : Lonavala

Sign

Dohudhay